

AMENDMENTS TO THE CLAIMS

Please add new claims 2-19 as follows:

- 1 1. (original) A method of reading data from a synchronous content addressable memory
2 (CAM) device, comprising the steps of:
3 instructing the CAM device to compare comparand data with data stored in a plurality of
4 first CAM cells;
5 comparing the comparand data with the data stored in each of the plurality of first CAM
6 cells;
7 sensing data stored in a second CAM cell; and
8 outputting the sensed data from the CAM device, wherein the instructing, comparing,
9 sensing, and outputting steps all occur in one clock cycle.
- 1 2. (new) The method of claim 1 wherein comparing the comparand data with the data stored
2 in each of the plurality of first CAM cells comprises providing the comparand data to the
3 plurality of first CAM cells via a plurality of compare lines.
- 1 3. (new) The method of claim 2 wherein sensing data stored in a second CAM cell comprises
2 receiving data in a sense amplifier coupled to the second CAM cell via at least one bit line.
- 1 4. (new) The method of claim 3 wherein the CAM device comprises an array of CAM cells
2 that includes the plurality of first CAM cells and the second CAM cell.
- 1 5. (new) The method of claim 3 wherein the plurality of first CAM cells includes the second
2 CAM cell.

- 1 6. (new) The method of claim 1 wherein sensing data stored in the second CAM cell
2 comprises addressing a row of CAM cells that includes the second CAM cell.
- 1 7. (new) The method of claim 6 wherein addressing a row of CAM cells that includes the
2 second CAM cell comprises addressing a row of CAM cells indicated by a match address
3 generated in a prior compare operation within the CAM device.
- 1 8. (new) The method of claim 1 wherein addressing the row of CAM cells indicated by a
2 match address generated in a prior compare operation within the CAM device comprises:
3 generating the match address within a priority encoder of the CAM device;
4 providing the match address from the priority encoder to an address decoder of the CAM
5 device; and
6 decoding the match address within the address decoder to activate a word line coupled to
7 the row of CAM cells.
- 1 9. (new) The method of claim 8 wherein providing the match address from the priority
2 encoder to the address decoder comprises latching the match address in an address latch
3 and outputting the match address from the address latch to the address decoder.
- 1 10. (new) The method of claim 8 wherein providing the match address from the priority
2 encoder to the address decoder comprises outputting the match address from the priority
3 encoder to an address selector and configuring the address selector to pass the match
4 address to the address decoder.
- 1 11. (new) The method of claim 10 wherein configuring the address selector to pass the match

address to the address decoder comprises asserting a control signal to the address selector in response to an instruction received from an external device.

12. (new) A synchronous content addressable memory (CAM) device comprising:

an array of CAM cells;

circuitry to compare first comparand data with contents of the array of CAM cells during a first clock cycle;

circuitry to sense data stored in a selected row of CAM cells within the array of CAM cells during the first clock cycle; and

circuitry to output the sensed data from the CAM device during the first clock cycle.

13. (new) The synchronous CAM device of claim 12 wherein the circuitry to compare first

comparand data with contents of the array of CAM cells comprises an instruction decoder

to receive an instruction to compare the first comparand data with the contents of the array of CAM cells.

14. (new) The synchronous CAM device of claim 12 wherein the array of CAM cells

comprises a plurality of columns of CAM cells, and wherein the circuitry to compare first

comparand data with contents of the array of CAM cells comprises a plurality of compare

lines coupled to a plurality of columns of CAM cells, and wherein the circuitry to sense

data stored in the selected row of CAM cells comprises a plurality of bit lines coupled to

the plurality of columns of CAM cells.

15. (new) The synchronous CAM device of claim 12 further comprising match circuitry,

including a priority encoder, to generate a match address based upon a comparison of

3 second comparand data with contents of the array of CAM cells.

1 16. (new) The synchronous CAM device of claim 15 wherein the circuitry to sense data stored
2 in a selected row of CAM cells comprises address decoding circuitry coupled to receive the
3 match address from the match circuitry and configured to decode the match address to
4 enable access to the selected row of CAM cells.

1 17. (new) The synchronous CAM device of claim 16 wherein the address decoding circuitry
2 comprises an address selector to select the match address from among a plurality of address
3 sources.

1 18. (new) A synchronous content addressable memory (CAM) device comprising:
2 an array of CAM cells;
3 means for comparing first comparand data with contents of the array of CAM cells during a
4 first clock cycle;
5 means for sensing data stored in a selected row of CAM cells within the array of CAM
6 cells during the first clock cycle; and
7 means for outputting the sensed data from the CAM device during the first clock cycle.

1 19. (new) The synchronous CAM device of claim 18 further comprising means for generating
2 a match address based upon a comparison of second comparand data with contents of the
3 array of CAM cells, and wherein the means for sensing data stored in the selected row of
4 CAM cells comprises means for decoding the match address to enable access to the
5 selected row of CAM cells.